Jiajian Luo

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SUMMARY

R&D Thermal Engineer at Cooler Master; ex-NVIDIA research intern; Ph.D. in electronic cooling; expertise in thermal management, liquid-cooling products, hands-on experiment, FEM/CFD, coding and ML optimization.

Skills

- Data-center thermal product design, manufacturing and commissioning (cold plate, CDUs).
- Semiconductor packaging (2.5D/3D packaging, CPO) and chip-level thermal management (photonics, TSV, TIMs, heat pipe, vapor chamber, heat sink).
- Cleanroom microfabrication and process engineering (lithography, metallization, etching, SEM)
- FEM/CFD simulation (OpenFOAM, ANSYS, COMSOL) and CAD software (Solidwords, Creo, FreeCAD)
- Thermal experiment and data acquisition automation (IR camera, thermocouples, RTDs).
- Coding, machine learning, and software development (python, C).
- English (fluent); Mandarin (native); Cantonese (native); Korean (intermediate)

EXPERIENCE

Thermal Engineer *Feb. 2026 –PRESENT*

Cooler Master, R&D Department, Fremont, CA

- Led the development of a thermal-hydraulic laboratory, including equipment sourcing, instrumentation, and workflow automation using chillers, pumps, thermal test vehicles (TTVs), sensors, and DAQ systems; conducted thermal/pressure DOEs for cold plates, manifolds, and CDUs.
- Led the thermal design of a data-center liquid-cooling product, including system architecture, component selection, BOM development, prototyping, CFD analysis, and experimental validation.
- Researched 3D-printed microchannel cold-plate optimization by modifying OpenFOAM-based source code and developing an adjoint-based sensitivity analysis CHT/CFD framework for topology optimization.
- Supported the manufacturing and commissioning of data-center liquid-cooling products, including CDUs, manifolds, and cold plates; contributed to customer-facing activities such as failure analysis and on-site technical support.

Research Intern *Jun. 2025 – Sep. 2025*

NVIDIA, Circuits Research Group, Santa Clara, CA

- Performed thermal simulations (ANSYS Icepak & Flotherm) for 2.5D/3D packaging, co-packaged optics, HBMs, and GPU/ASIC systems, identifying design trade-offs.
- Designed and benchmarked advanced cooling methods for next-gen photonics-enabled GPUs, including thermoelectric, microchannel, and TIM-based solutions.
- Collaborated cross-functionally with photonic and electrical engineers, providing thermal insights that informed design integration and improved system performance.

Graduate Researcher *Sep. 2019 – Sep. 2025*

Department of Mechanical and Aerospace Engineering, UC Irvine, CA

- Developed nanoscale thermoelectric coolers for chip-level thermal management, achieving an 8 °C cooling under a 400 W/cm², 100 × 100 μm² hotspot.
- Conducted cleanroom microfabrication processes including lithography, metal deposition, lift-off, and etching to fabricate experimentally functional in-chip TEC devices.
- Built automated thermal-electrical experimental platforms with GPIB-controlled instrumentation, DAQ integration, RTD/thermocouple sensing, IR thermography, and vacuum-based testing for transient and steady-state thermal characterization and simulation validation.
- Developed ML-assisted optimization algorithm for chip- and system-level thermal control using supervised learning (NN, CNN, LSTM) and reinforcement learning (DQN).

PUBLICATION

1. **Luo, J.** and Lee J. "Machine Learning-Assisted Thermoelectric Cooling for Multi-Hotspot Dynamic Thermal Management." *Journal of Applied Physics* (2024) https://doi.org/10.1063/5.0206287
2. **Luo, J.** et al. "Dynamic Thermal Management in SOI Transistors Using Holey Silicon-Based Thermoelectric Cooling." *IEEE Transactions on Electron Devices* (2024) https://doi.org/10.1109/TED.2024.3358788
3. **Luo, J.** et al. "Thermal Management of SOI-Based Devices Using Holey Silicon-Based Lateral Thermoelectric Cooler." ASME Heat Transfer Summer Conference (2024) https://doi.org/10.1115/HT2024-122922
4. **Luo, J.** et al. " Dynamic Thermal Management of Power Transistors using Holey Silicon-Based Thermoelectric Cooling." The 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (2021) https://doi.org/10.1109/iTherm54085.2022.9899681
5. **Luo, J.** et al. "Analysis of Non-Fourier Heat Conduction Problem with Suddenly Applied Surface Heat Flux." *Journal of Thermophysics and Heat Transfer* (2020) https://doi.org/10.2514/1.T5849

EDUCATION

University of California, Irvine, CA, USA

- *Ph.D. in Mechanical Engineering* (GPA: 3.9/4.0) *Sep. 2019 – Dec. 2025*

Wuhan University, Wuhan, Hubei, China

- *B.ENG in Hydraulic Power Engineering* (GPA: 3.2/4.0) *Sep. 2014 – Jun. 2018*